REMARKS

The objections to the specification have been corrected. The claim objections have been corrected.

With respect to the § 112 objections, all the corrections in paragraph A have been corrected.

With respect to the objection in paragraph B, the "issue latency", "issue latency" is defined in the specification at page 5, lines 7 and 8 as "the number of cycles between start of two adjacent instructions".

With respect to the objection to claim 5, it is not believed there is any inconsistency. The claim is clear that it is from start to end of the issue of the first and second instructions. There is no requirement that claim 5 relate to assigning a number of stall cycles.

Claim 7 has been amended to remove the issue.

Objections to claims 8 and 9 have been corrected by amendment.

With respect to the objection the claim 17, there is no requirement that claim 17 be related to assigning a number of stall cycles. Therefore reconsideration is requested.

Claim 1 has been amended to call for determining a range within which one of said instructions can be reordered without violating data dependency and reordering said instruction within that range.

Support for the added limitation may be found in the specification at page 6, lines 9-14.

Nothing of the sort is discussed in the cited reference and therefore reconsideration is respectfully requested.

The other independent claims have been amended similarly.

Respectfully submitted,

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Timothy N. Trop, Reg. No. 28,994
TROP, PRUNER & HU, P.C.
1616 S. Voss Road, Suite 750
Houston, TX 77057
713/468-8880 [Phone]
713/468-8883 [Fax]